REMARKS

The Examiner is thanked for the clearly stated action. This communication is filed in response to the Office Action having a mailing date of June 8, 2009, in which a three (3) month Shortened Statutory Period for Response has been set, due to expire September 8, 2009 . Twenty-three (23) claims, including three (3) independent claims, were paid for in the application. Claims 1, 5, 10, 21, and 23 are currently amended. Claim 4 is canceled. No new matter has been added to the application, and all claims are believed in condition for allowance. Upon entry of the amendments herewith, claims 1-3 and 5-23 remain pending. Reconsideration of the present application in view of the following remarks is respectfully requested.

I. Objections to Claim 21

The Office Action, at Page 2, objects to claim 21 for multiple recitations of the "host controller." As suggested by the Examiner, the third recitation of the "host controller" has been amended to recite the "host microprocessor," consistent with he originally filed specification at Page 4, Lines 23-35. The Examiner is thanked for identifying this typographical error, which is now corrected. Withdrawal of the objection is respectfully requested.

II. Telephone Interview Summary

A telephone interview was held between the attorney of record (Thomas J. Satagaj) and the Examiner on July 20, 2009. An Interview Summary form PTOL-413 mailed on July 24, 2009 indicated that the present amendment/response must include "the substance of the interview." Accordingly, the substance of the interview is provided below:

Mr. Satagaj and the Examiner discussed the cited references and certain features in the claims by telephone on April 18, 2009. No agreement on the allowability on the claims was reached in the telephone conversation, but the Examiner did recommend amending the independent claims to reflect subject matter of Page 4, Lines 21-22 of the originally filed specification, which discusses memory mapping transfer-based descriptors.

III. Rejections under 35 U.S.C. § 103(a)

The Office Action once again maintained rejections of all claims under 35 U.S.C. § 103(a) as allegedly unpatentable over ***Wang et al.*, (U.S. Appl. 2002/0116565)**, hereinafter *Wang*, in view of ***Hamdi et al.*, (U.S. Pat. 6,912,651)**, hereinafter *Hamdi*.

a. Independent Claim 1; memory mapped payload

In accordance with the Examiner's recommendations, claim 1 has been amended. Originally filed claim 4, which had at least some parts of the amended claim language, has been canceled. Amended claim 1 now recites, *inter alia*, "an internal memory configured into at least two distinct sections to store a plurality of transfer-based transfer descriptors including a first section configured to store a plurality of transfer-based transfer descriptor headers, and a second section configured to store a plurality of transfer-based transfer descriptor payloads, the respective transfer-based transfer descriptors received through the first interface, said internal memory having a plurality of transfer-based transfer descriptor header and transfer-based transfer descriptor payload locations mapped in the host microprocessor."

Accordingly, the internal memory of the host controller has an address space configured into distinct header and payload areas, and the header and payload areas of the internal memory are directly accessible by the host microprocessor. In this way, the host microprocessor may read data from and write data to the host controller internal memory via the direct connection of the internal memory through the first interface. Support for this feature is found in the International publication of the present application, WO 2004/102406 A1, at least in Figures 2 and 3 and on Page 4, Lines 18-22. For at least the reason that neither *Wang* nor *Hamdi*, alone or in any motivated combination, show this feature, claim 1 is in condition for allowance.

b. Independent Claim 1; *Wang* does not have memory mapped payload

In *Wang*, memory transactions are triggered via an interrupt asserted by the host controller. *Wang's* host microprocessor acts on the interrupt and proceeds to copy data between system memory 32 and batch memory 30. See *Wang's* FIG. 1A and Para. [0042-0043].

Nevertheless, there is no indication that *Wang's* host controller 22 and his host microprocessor 24 share memory address space such that a plurality of transfer descriptor header and transfer descriptor payload locations are mapped in the host microprocessor 24. Instead, Paragraphs [0138-0141] of *Wang* describe the mechanism of *Wang's* data transfer.

In a bus mastering host controller, such as required by standard OHCI or UHCI driver running on a host microprocessor, the host controller will take control of the bus and copy data directly to and from a host microprocessor's system memory. Neither *Wang* nor claim 1 has bus mastering capability. Instead, claim 1 requires an "internal memory having a plurality of transfer-based transfer descriptor header and transfer-based transfer descriptor payload locations mapped in the host microprocessor," and *Wang* requires an interrupt driven USB Engine 168 to spoof the standard OHCI or UHCI driver running on a host microprocessor into thinking that the host controller has bus mastering capability. See *Wang's* Paragraph [0139]. Paragaph [0141] of *Wang* further describe the functionality of the USB Engine 168 to make use of both shared memory in the host microprocessor (not in the host controller) and/or use of control registers (not memory mapped memory) in the host controller. Accordingly, since there is no disclosure, teaching, or suggestion that *Wang's* host controller has "internal memory having a plurality of transfer-based transfer descriptor header and transfer-based transfer descriptor payload locations mapped in the host microprocessor," claim 1 is in condition for allowance.

c. Independent Claim 1; *Hamdi* does not have mapped memory

As discussed in a previous response, *Hamdi* does not supply the missing features of claim 1 to cure the deficiency of *Wang*. This is further true in light of the amendments made to claim 1. Once again, *Hamdi* is a conventional USB system that merely provides for host controller 608 to master bus 604 and access RAM 606. See *Hamdi's* FIG. 6 and Col. 11, lines 41-64. There is no indication that *Hamdi's* host controller 608 and his microprocessor 602 share any memory address space in different memory devices. Thus, there is no indication that *Hamdi's* host controller 608 has any internal memory having a plurality of "transfer-based transfer descriptor header and transfer-based transfer descriptor payload" locations mapped to the microprocessor 602. Accordingly, claim 1 is allowable over *Hamdi*.

d. Independent Claim 1; *Hamdi* and *Wang* ought not be combined

In addition to the reasons that claim 1 is allowable over the individually cited references, a previous response also discussed why claim 1 is further allowable over a combination of *Wang* and *Hamdi*. In the previous response, it was put forth that claim 1 is allowable for at least the reason that *Wang* and *Hamdi* could not be joined in such a way as to form operable device.

MPEP § 2143 provides examples of basic requirements for showing a prima facie case of obviousness via a combination of references. Taking a cue from *KSR v. Teleflex*, 550 U.S. 398 (2007), MPEP § 2143 lays out seven exemplary rationales that may support a conclusion of obviousness. Rationale (A) describes combining prior art elements according to known methods to yield predictable results. Rationale (B) describes simple substitution of disclosed elements. Neither of rationales (A) and (B) is applicable here because, as discussed herein and in a previous response, simply adding the direct bus connection of *Hamdi* to *Wang* would create a very unpredictable, non-functioning device.

None of rationales (C) – (F) are applicable here for apparent reasons.

Rationale (G) in MPEP § 2143 describes teaching, suggestion, and motivation to combine references. *Hamdi* describes a conventional USB bus mastering host controller, and *Wang* mentions at Paragraph [0138] that such a system is incompatible with his invention. Accordingly, since *Wang* expressly teaches that such configuration is incompatible, the references ought not to be combined.

The above rationale for not combining *Wang* and *Hamdi* not withstanding, the present Office Action, at Page 5 suggests that none of *Hamdi's* functionality would be incorporated but merely the direct connection of *Hamdi's* memory on the microprocessor memory bus. This is incorrect because the only reason *Hamdi* has the direct connection is because of his bus mastering capability. The operation of *Hamdi* to use the direct connection cannot be separated from the direct connection. That is, if *Hamdi* does not have a direct connection, his device will not operate. If *Wang* merely adds *Hamdi's* direct connection without his bus mastering capability, then *Wang* will fail to operate because *Wang's* own host controller

could not access the host controller memory (now placed on the system bus) without risk of collisions with memory accesses by the host microprocessor.

With respect to motivation to combine references, MPEP §§ 2143.01.III-VI describe how incompatible configurations should not be relied on to find obviousness. Especially MPEP § 2143.01 VI, entitled "The Proposed Modification Cannot Change the Principle of Operation of the Reference," is noted. In the present case, since combining *Hamdi* with *Wang* will change the principle of operation of *Wang* into an incompatible configuration, a combination of *Wang* with *Hamdi* is inappropriate, and claim 1 should be allowed.

e. Independent Claim 10

Claim 10 has been amended with similar recitations as amended claim 1. It is further apparent that even though the language of claim 10 is not identical to that of claim 1, the nonobviousness of claim 10 will be apparent in view of the above remarks. For example, claim 10 recites, *inter alia*, "an internal memory, for storing a plurality of transfer-based transfer descriptors, the transfer descriptors including header and payload, received through the first interface, said internal memory having a plurality of header and payload transfer descriptor locations mapped in the host microprocessor." As discussed above, neither *Wang* nor *Hamdi*, alone or combined, have a host controller with memory including a plurality of "payload transfer descriptor locations" mapped in a host microprocessor. Accordingly, claim 10 is in condition for allowance.

f. Independent Claim 23

Independent claim 23 recites, *inter alia*, "configuring header and payload transfer-based transfer descriptor address space of an internal memory to be mappable in the host microprocessor, said address space accessible via the memory bus," and "configuring the internal memory to store a plurality of header and payload transfer-based transfer descriptors received via the memory bus." As discussed herein, none of the cited references permit configuration of a host controller as a slave on the memory bus such that an internal memory of the host controller,

including "payload transfer-based transfer descriptor address space" is mappable in the host processor. Claim 23 is thus in condition for allowance.

IV. Conclusion

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim. If the attorney of record (Thomas J. Satagaj) has overlooked a teaching in any of the cited references that is relevant to the patentability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact Mr. Satagaj at (206) 622-4900.

The Director is authorized to charge any additional fees due by way of this Amendment only, or credit any overpayment, to our Deposit Account No. 19-1090. Reconsideration of the present application in view of the foregoing amendments and the following remarks is respectfully requested. A Notice of Allowance is earnestly solicited.

Respectfully submitted,

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